

"AUTOMATED 800 LEARNING SEQUENCE" FLOW MODEL

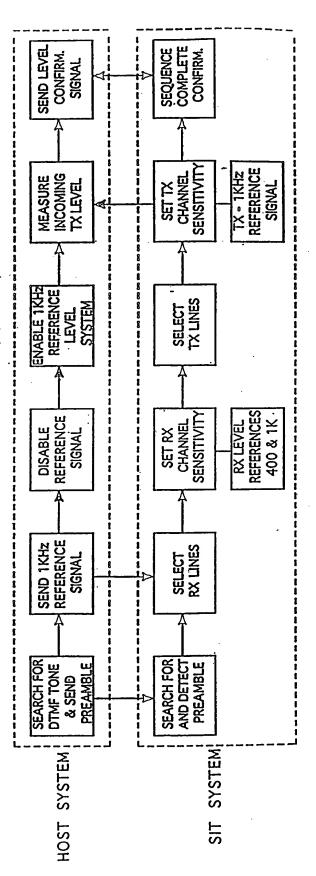
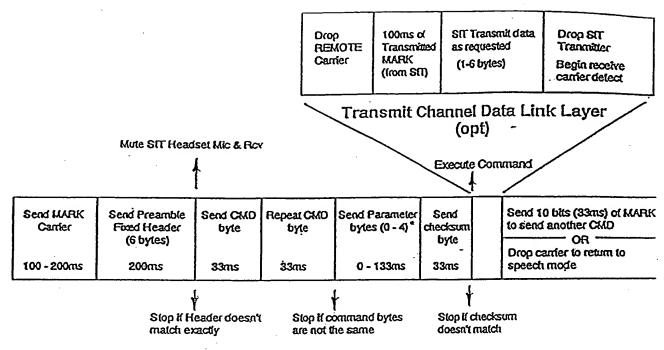
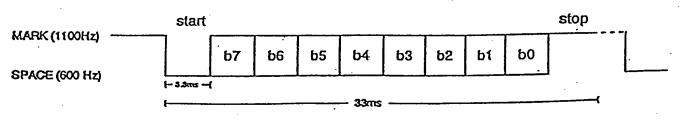


FIG. 2



NOTE: The number of parameters is directly dependent on the Command type

Receive Channel Data Link Layer



Receive Channel Physical Layer

FIG. 3

Smart Interface Technology (SIT) Project Preliminary Line Configuration Switching Algorithms and Model

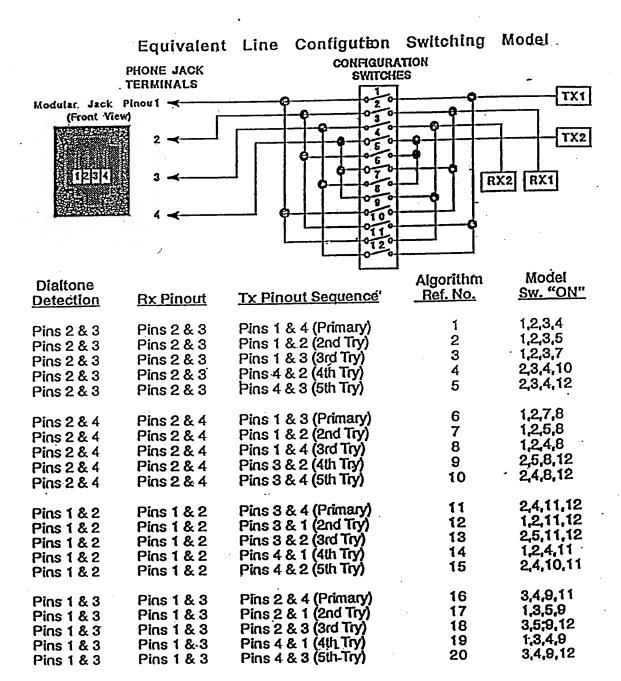


FIG. 4

Diattone <u>Detection</u>	Rx Pinout	Tx Pinout Sequence	Algorithm <u>Ref. No.</u>	Model Sw. "ON"
Pins 1 & 4	Pins 1 & 4 Pins 1 & 4 Pins 1 & 4 Pins 1 & 4 Pins 1 & 4	Pins 2 & 3 (Primary) Pins 2 & 1 (2nd Try) Pins 2 & 4 (3rd Try) Pins 3 & 1 (4th Try) Pins 3 & 4 (5th Try)	21 22 23 24 25	7,8,9,10 1,5,8,9 4,8,9,10 1,7,8,9 4,8,9,12
Pins 3 & 4 Pins 3 & 4 Pins 3 & 4 Pins 3 & 4 Pins 3 & 4	Pins 3 & 4 Pins 3 & 4 Pins 3 & 4 Pins 3 & 4 Pins 3 & 4	Pins 1 & 2 (Primary) Pins 1 & 3 (2nd Try) Pins 1 & 4 (3rd Try) Pins 2 & 3 (4th Try) Pins 2 & 4 (5th Try)	26 27 28 29 30	1,3,5,6 1,3,6,7 1,3,4,6 3,6,7,10 3,4,6,10

ALGORITHM REF, NUMBER	SWITCHING MODEL ACTION	ALGORITHM TREF. NUMBER	SWITCHING MODEL ACTION
31	Switch 1: "ON"	43	Switch 7: "ON"
32	Switch 1: "OFF"	4,4	Switch 7: "OFF"
33	Switch 2: "ON"	45	Switch 8: "ON"
34	Switch 2: "OFF"	46	Switch 8: "OFF"
35	Switch 3: "ON"	47	Switch 9: "ON"
3 6 ·	Switch 3: "OFF"	48	Switch 9: "OFF"
37	Switch 4: "ON"	49	Switch 10: "ON"
38	Switch 4: "OFF"	50	Switch 10: "OFF"
39	Switch 5: "ON"	.51	Switch 11: "ON"
40	Switch 5: "OFF"	52	Switch 11: "OFF"
41	Switch 6: "ON"	53 -	Switch 12: "ON"
42	Switch 6: "OFF"	54	Switch 12: "OFF"

NOTES:

Algorithm No. 1 will be the default setting for system power-up, hard or soft resets and "learning" timeout conditions.
 Ideally all 12 equivalent switches can be selected and switched "on" or "off" independant of the above algorithm's.

FIG. 5

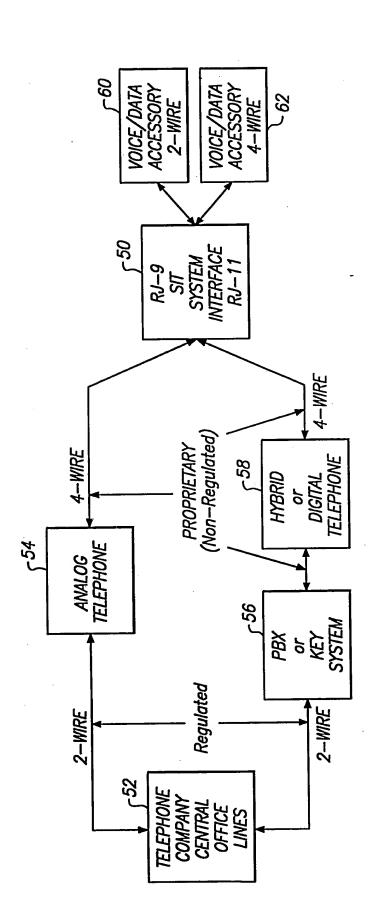


FIG. 6

SIT FULL

SIT MCU

RX1 OUT

P8 P9 P10

2228

SERIAL

EEPROM

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P11

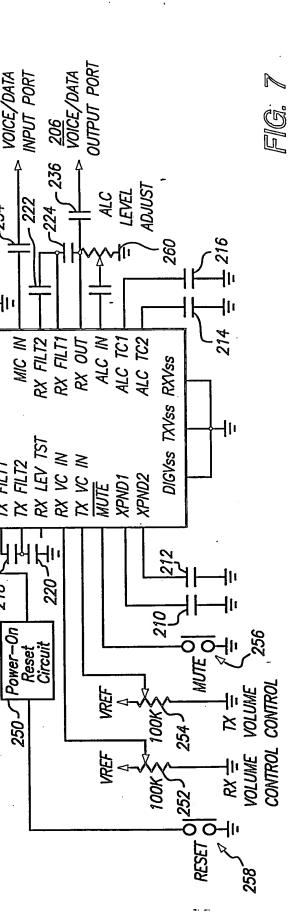
MODE/ENABLE DATA OUT

<u>204</u> VOICE/DATA INPUT PORT

TX2 RET

A/D IN TONE OUT RESET

401



COMBEND CHORD

200

VCC SLEEP

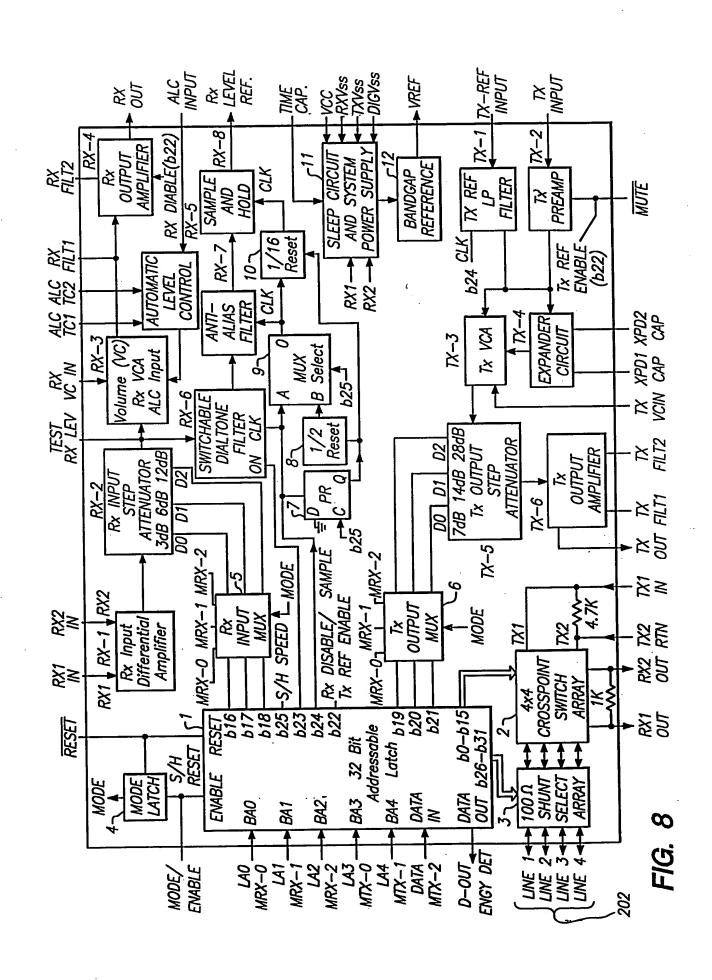
VREF

VREF

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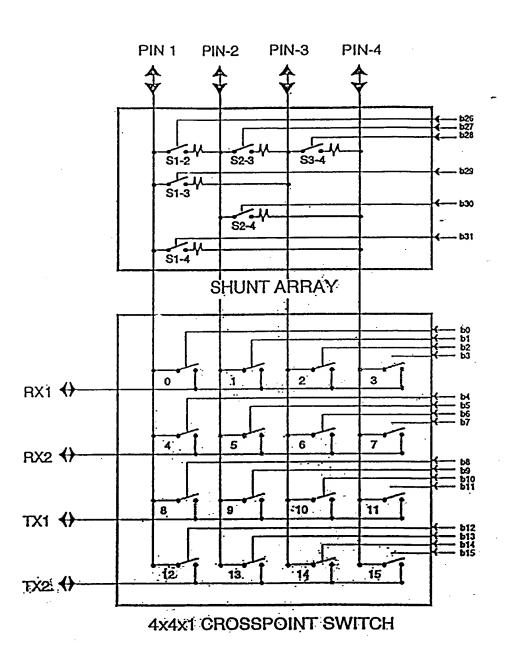


FIG. 9